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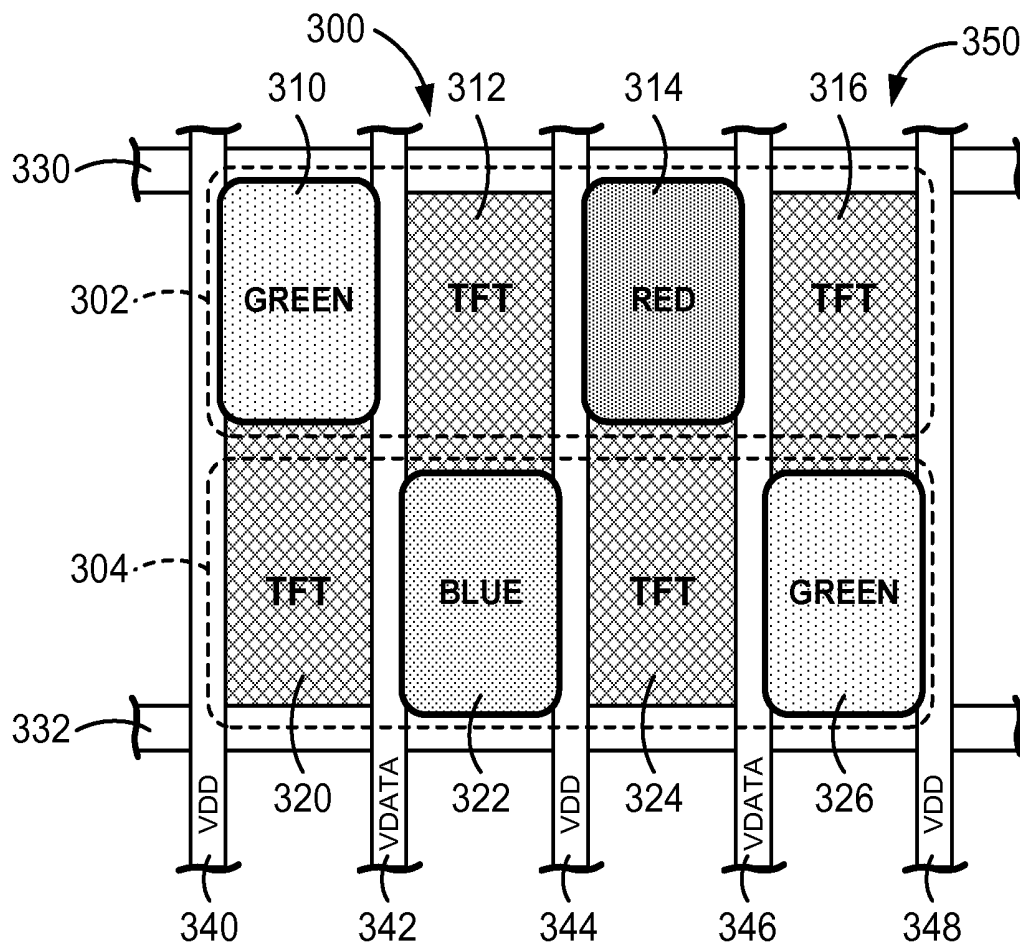
(63) Continuation of application No. 13/724,424, filed on Dec. 21, 2012, now Pat. No. 8,803,417, which is a continuation-in-part of application No. 12/958,035, filed on Dec. 1, 2010, now Pat. No. 8,552,636.

Foreign Application Priority Data

Dec. 1, 2009 (CA) 2686174

(57) **ABSTRACT**

A pixel structure comprises a substantially transparent substrate, a drive transistor formed on the substrate, an organic light emitting device formed on the opposite side of the drive transistor from the substrate, a reflective layer disposed between the light emitting device and the drive transistor and having a reflective surface facing the light emitting device. The reflective layer forms an opening offset from the drive transistor for passing light emitted by the light emitting device to the substrate. At least a portion of the reflective layer is preferably concave in shape to direct reflected light from the light emitting device back onto the light-emitting device.



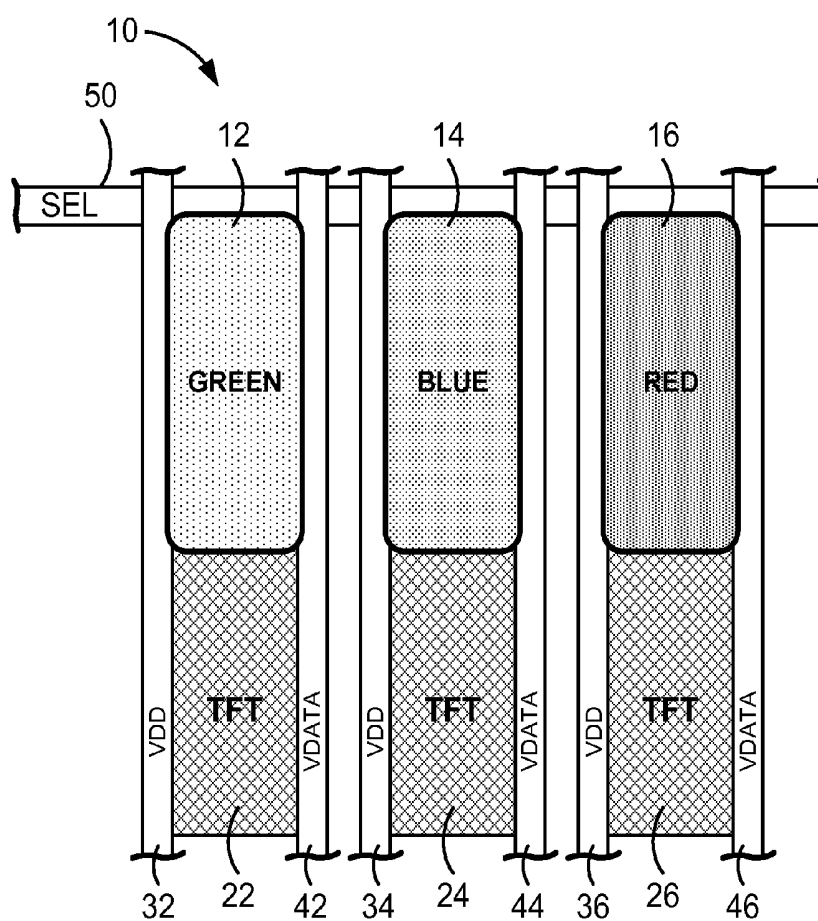


FIG. 1A
(PRIOR ART)

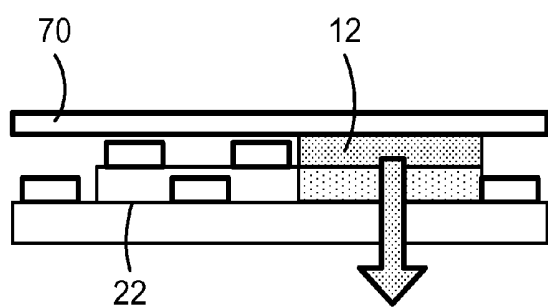


FIG. 1C
(PRIOR ART)

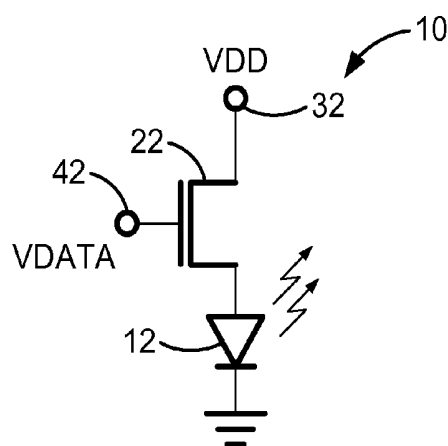


FIG. 1B
(PRIOR ART)

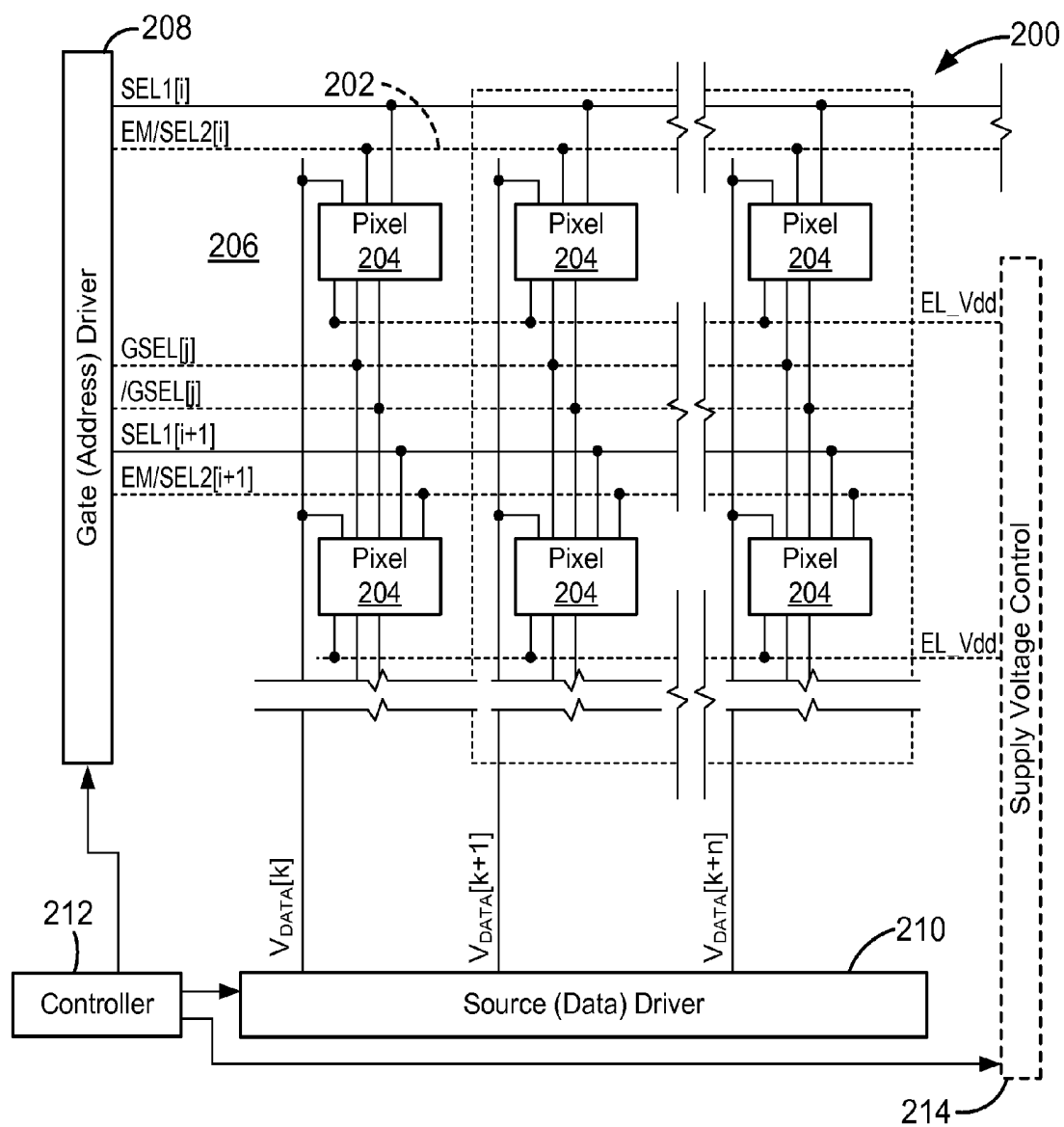


FIG. 2

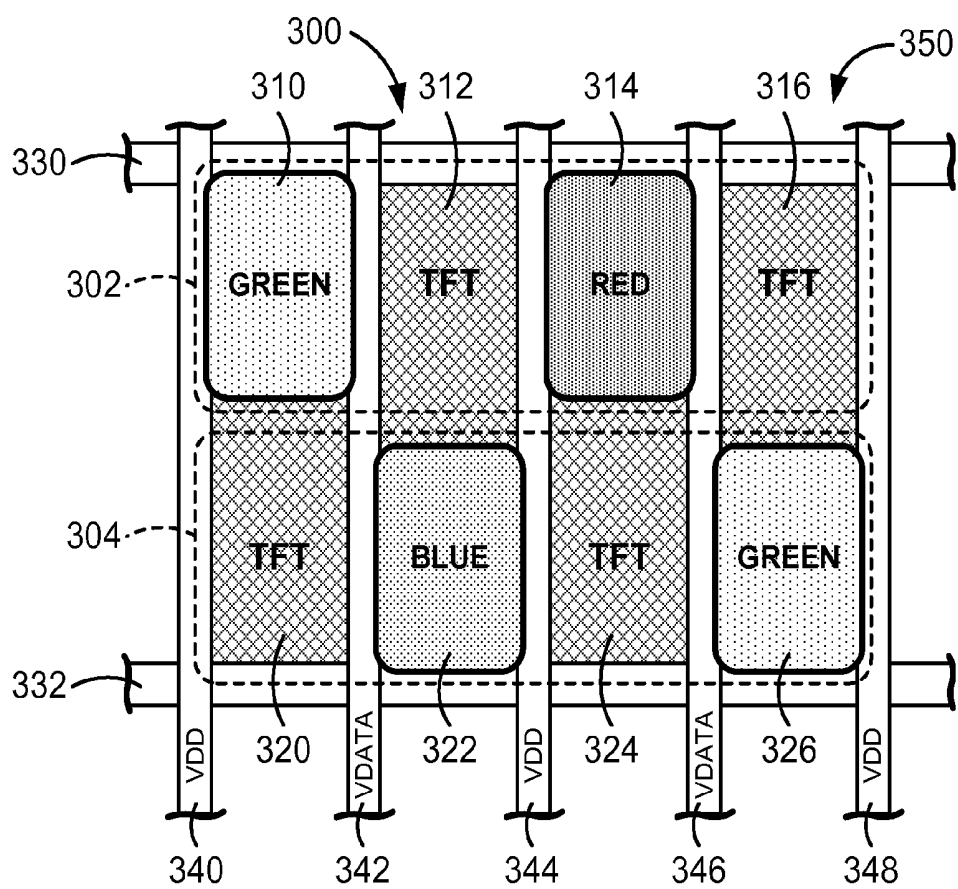


FIG. 3

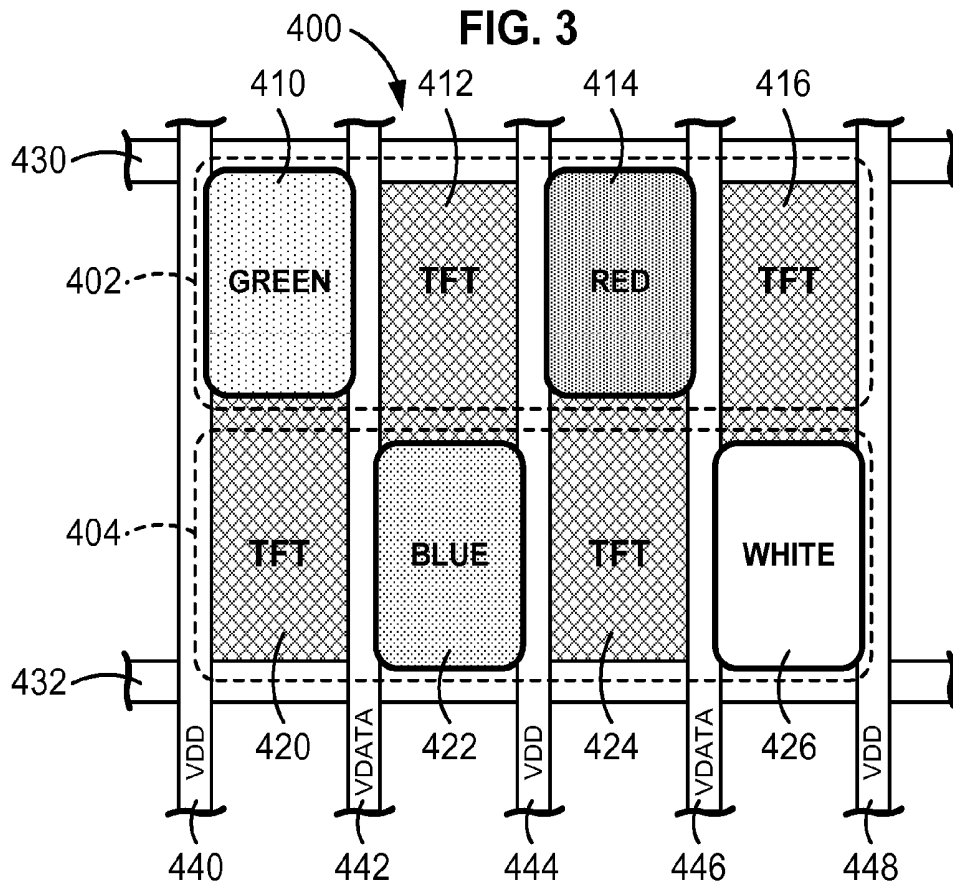


FIG. 4

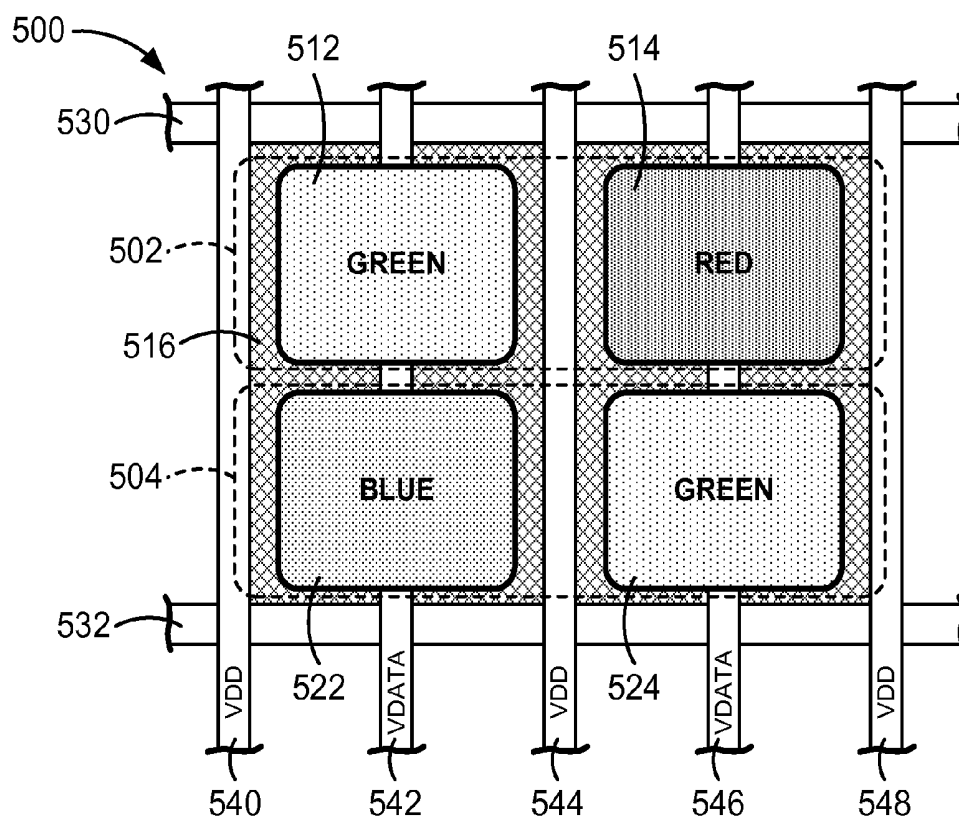


FIG. 5

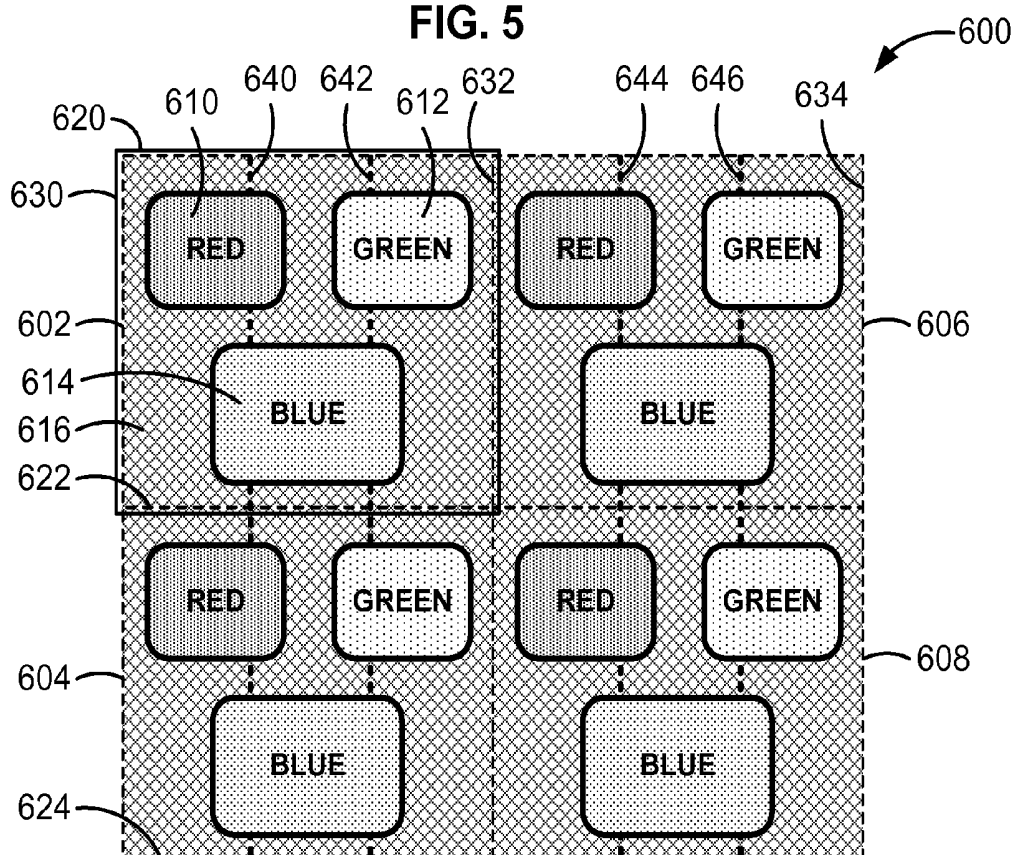


FIG. 6

FIG. 7

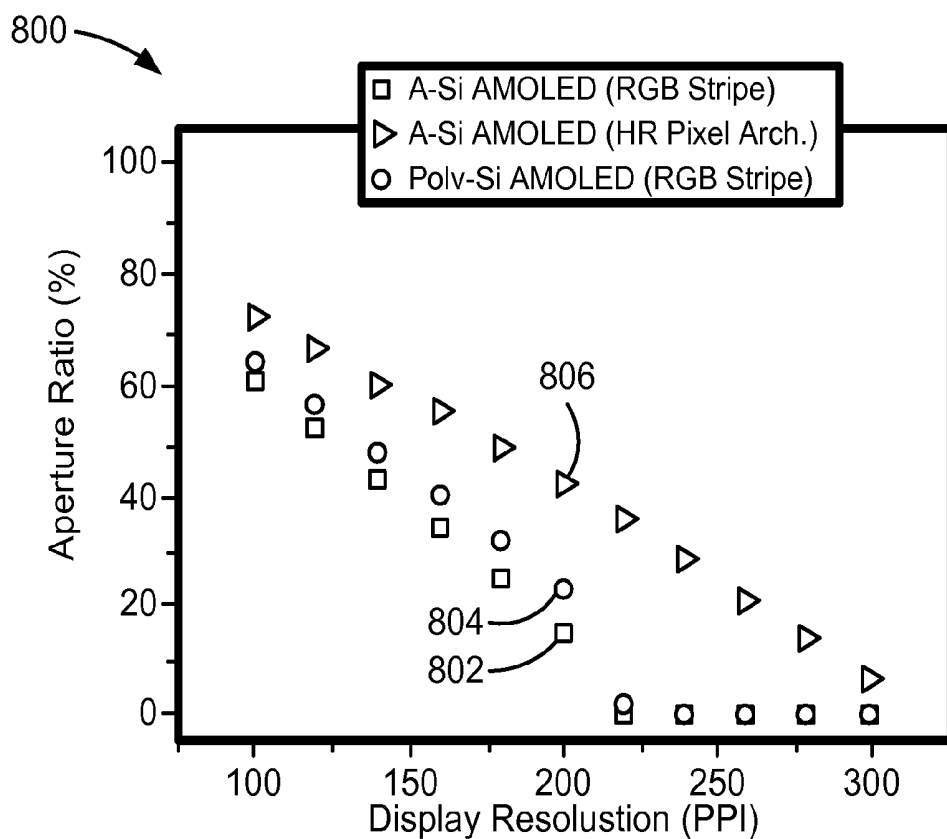


FIG. 8A

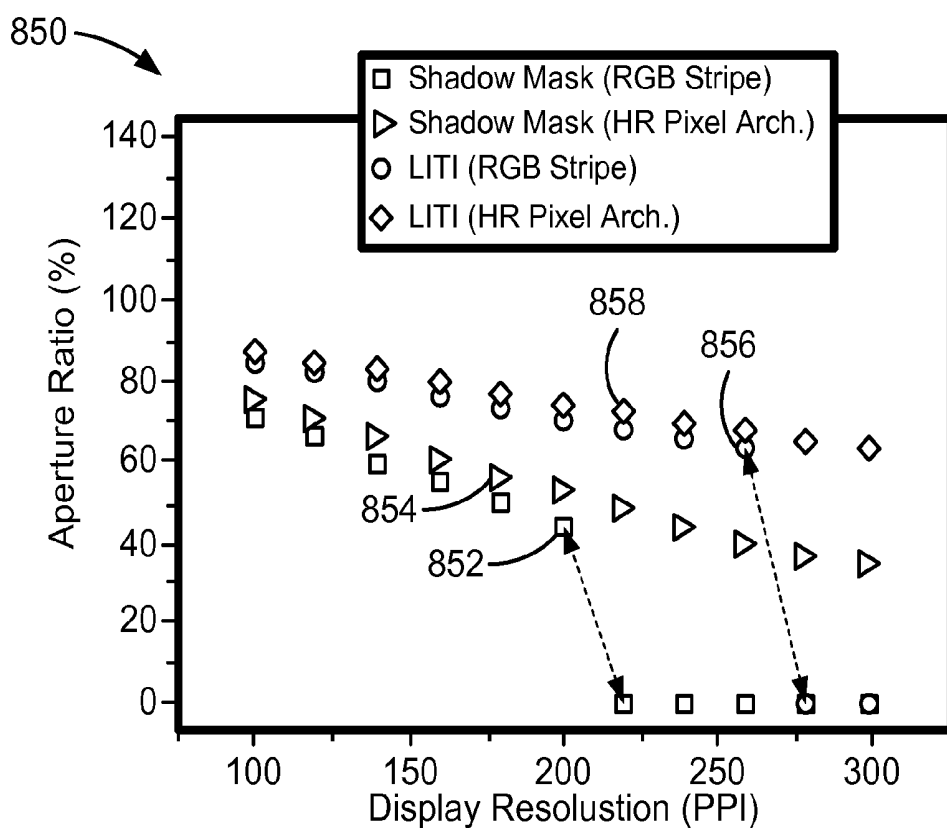


FIG. 8B

FIG. 9a

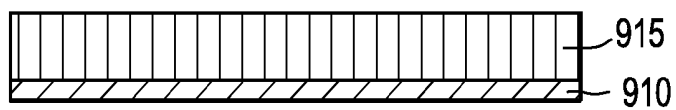


FIG. 9b

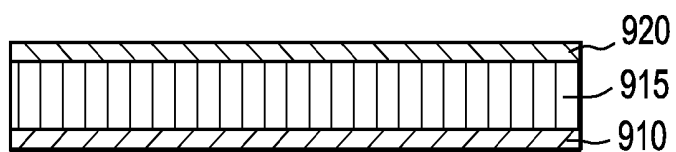


FIG. 9c

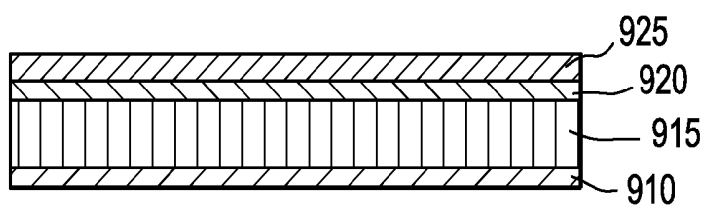


FIG. 9d

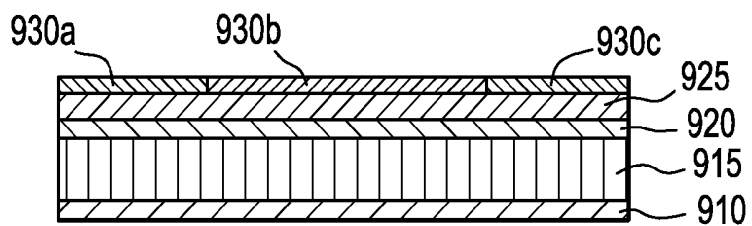


FIG. 9e

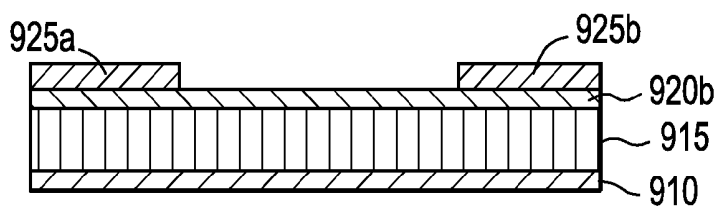


FIG. 9f

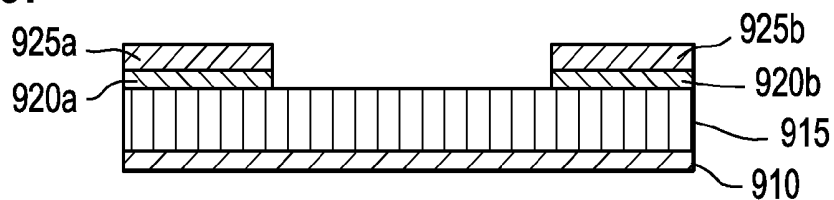


FIG. 9g

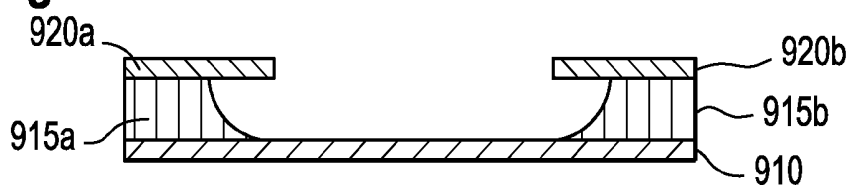


FIG. 9h

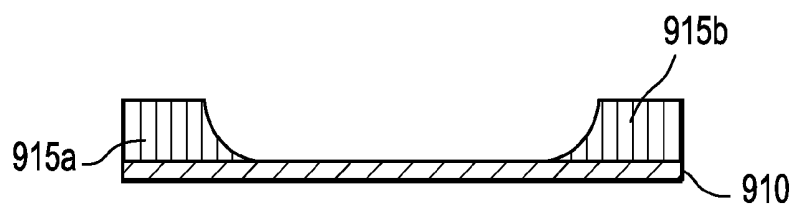


FIG. 9i

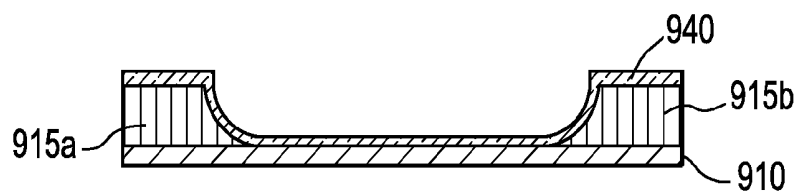


FIG. 9j

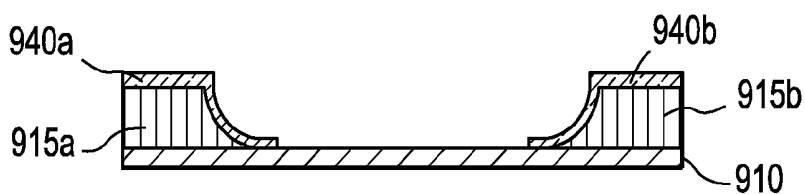


FIG. 9k

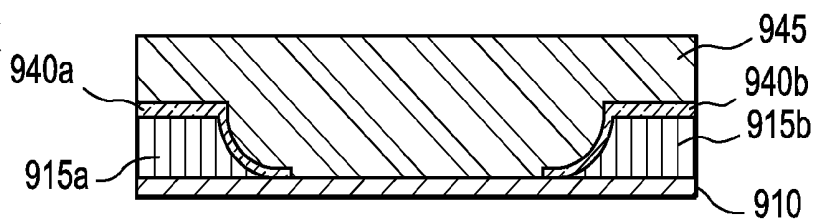


FIG. 9l

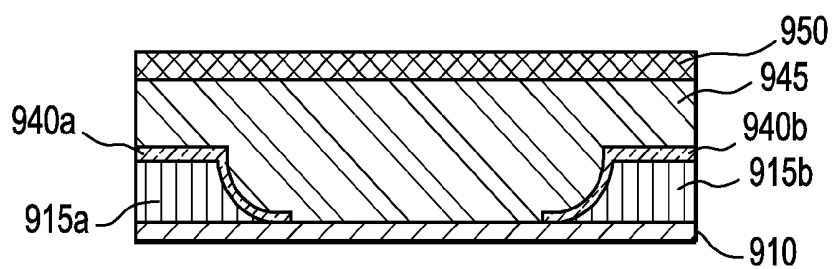
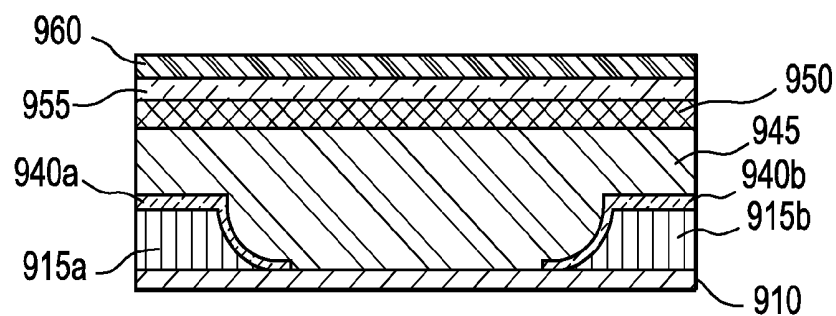


FIG. 9m



HIGH RESOLUTION PIXEL ARCHITECTURE

CROSS-REFERENCE TO RELATED APPLICATION(S)

[0001] This application claims priority to, and is a continuation-in-part of, U.S. application Ser. No. 12/958,035, filed Dec. 1, 2010, which is herein incorporated by reference in its entirety. This application further claims priority to Canadian Application No. 2,686,174, which was filed Dec. 1, 2009, herein incorporated by reference in its entirety.

FIELD OF THE INVENTION

[0002] The present invention generally relates to active matrix organic light emitting device (AMOLED) displays, and particularly to a pixel structure that has a larger aperture ratio in such displays.

BACKGROUND

[0003] Currently, active matrix organic light emitting device ("AMOLED") displays are being introduced. The advantages of such displays include lower power consumption, manufacturing flexibility and faster refresh rate over conventional liquid crystal displays. In contrast to conventional liquid crystal displays, there is no backlighting in an AMOLED display as each pixel consists of different colored organic light emitting devices (e.g., red, green and blue) emitting light independently. The organic light emitting diodes (OLED) emit light based on current supplied through a drive transistor. The drive transistor is typically a thin film transistor (TFT) fabricated from either amorphous silicon or polysilicon. The power consumed in each OLED has a direct relation with the magnitude of the generated light in that OLED.

[0004] The drive-in current of the drive transistor determines the pixel's luminance and the surface (aperture) of the actual OLED device determines the pixel's OLED lifetime. AMOLED displays are typically fabricated from the OLED, the drive transistor, any other supporting circuits such as enable or select transistors as well as various other drive and programming lines. Such other components reduce the aperture of the pixel because they do not emit light but are needed for proper operation of the OLED.

[0005] Generally color displays have three OLEDs arranged in a "stripe" for each pixel 10 as shown in FIG. 1A. The pixel 10 in FIG. 1A is a bottom emission type OLED where the OLEDs are fabricated on the substrate of the integrated circuit where there is no other components such as transistors and metal lines. The pixel 10 includes OLEDs 12, 14 and 16 and corresponding drive transistors 22, 24 and 26 arranged in parallel creating a "stripe" arrangement. Parallel power lines 32, 34 and 36 are necessary to provide voltage to the OLEDs 12, 14 and 16 and drive transistors 22, 24 and 26. The OLEDs 12, 14 and 16 emit red, green and blue light respectively and different luminance levels for each OLED 12, 14 and 16 may be programmed to produce colors along the spectrum via programming voltages input from a series of parallel data lines 42, 44 and 46. As shown in FIG. 1A, additional area must be reserved for a select line 50 and the data lines 42, 44 and 46 as well as the power lines 32, 34 and 36 for the OLEDs 12, 14 and 16 and the drive transistors 22, 24 and 26. In this known configuration, the aperture of the integrated circuit of the pixel 10 is much less than the overall area of the integrated circuit because of the areas needed for

the drive transistor and power and data lines. For example, in producing a shadow mask for fabricating such an integrated circuit for the pixel 10, the distance between two adjacent OLEDs such as the OLEDs 12 and 14 and the OLED size is significant (larger than 20 μm). As a result, for high resolution display (e.g. 253 ppi with 33.5 μm sub pixel width), the aperture ratio will be very low.

[0006] FIG. 1B shows a circuit diagram of the electronic components, namely the OLED 12, the drive transistor 22, the power input for the drive voltage line 32 and the programming voltage input 42 for each of the color OLEDs that make up the pixel 10. The programming voltage input 42 supplies variable voltage to the drive transistor 22 that in turn regulates the current to the OLED 12 to determine the luminance of the OLED 12.

[0007] FIG. 1C shows the cross section for the conventional bottom emission structure such as for the pixel 10 in FIG. 1A. As is shown, OLED 12 is fabricated to the side of the other components on the substrate in an open area. Thus, the OLED light emission area is limited by the other components in the pixel. A common electrode layer 70 provides electrical connection to the OLED 12. In this case, the current density is high because of the limited area for light emission. The OLED voltage is also high due to higher current density. As a result, the power consumption is higher and the OLED lifetime is reduced.

[0008] Another type of integrated circuit configuration for each of the OLEDs that make up the pixel involves fabricating the OLED over the backplane components (such as transistors and metal traces) and is termed a top emission configuration. The top emission configuration allows greater surface area for the OLED and hence a higher aperture ratio, but requires a thinner common electrode to the OLEDs because such an electrode must be transparent to allow light to be emitted from the OLEDs. The thin electrode results in higher resistance and causes significant voltage drop across this electrode. This may be an issue for larger area displays which in nature need a larger area common electrode.

[0009] Therefore, currently, the apertures of pixels for OLED displays are limited due to the necessity of drive transistors and other circuitry. Further, the aperture ratios of the OLEDs in OLED displays are also limited because of the necessity to have a minimal amount of space between OLEDs due to design rule requirements. Therefore, there is a need for increasing the aperture ratios of OLED based integrated circuit pixels for higher resolution displays.

SUMMARY

[0010] In accordance with one embodiment, a pixel structure comprises a substantially transparent substrate, a drive transistor formed on the substrate, an organic light emitting device formed on the opposite side of the drive transistor from the substrate, a reflective layer disposed between the light emitting device and the drive transistor and having a reflective surface facing the light emitting device, the reflective layer forming an opening offset from the drive transistor for passing light emitted by the light emitting device to the substrate. At least a portion of the reflective layer is preferably concave in shape to direct reflected light from the light emitting device back onto the light-emitting device.

[0011] In one implementation, the pixel structure comprises a substrate; a first photoresist layer having a first opening over the substrate; a reflective layer having a second opening, the reflective layer covering the first photoresist

layer; a second photoresist layer in the second opening and over the reflective layer; and an organic light emitting device formed over the second photoresist layer. The second opening overlaps with the first opening, and at least a portion of the reflective layer is concave in shape. A drive transistor is disposed between the substrate and the first photoresist layer for controlling the luminance of the organic light emitting device. The organic light emitting device preferably comprises an anode layer over the second photoresist layer, an organic electroluminescent layer over the anode layer, and a cathode layer over the organic electroluminescent layer. The reflective layer has a reflective surface facing the organic light emitting device, and directing light from the organic light emitting device to the second opening.

[0012] In accordance with another embodiment, a method of forming a pixel structure comprises providing a substrate; forming a first photoresist layer having a first opening over the substrate; forming a reflective layer having a second opening, the reflective layer covering the first photoresist layer; forming a second photoresist layer in the second opening and over the reflective layer; and forming an organic light emitting device over the second photoresist layer. The second opening overlaps the first opening, and at least a portion of the reflective layer is concave in shape. In one implementation, the step of forming the first photoresist layer comprises depositing the first photoresist layer on the substrate; forming a first mask layer on the first photoresist layer; depositing a third photoresist layer on the first mask layer; forming a second mask layer on the third photoresist layer; applying ultraviolet radiation to the second mask layer, thereby separating the third photoresist layer; removing the second mask layer; etching the first mask layer with the third photoresist layer, thereby separating the first mask layer; removing the third photoresist layer; etching the first photoresist layer with the first mask layer, thereby forming the first opening; and removing the first mask layer.

[0013] The step of forming the reflective layer preferably comprises depositing the reflective layer on the first photoresist layer and the substrate; depositing a third photoresist layer on the reflective layer; applying ultraviolet radiation to the third photoresist layer; developing the third photoresist layer; etching the reflective layer with the third photoresist layer, thereby forming the second opening; and removing the third photoresist layer.

[0014] The step of forming an organic light emitting device over the second photoresist layer preferably comprises forming an anode layer over the second photoresist layer; forming an organic electroluminescent layer over the anode layer; and forming a cathode layer over the organic electroluminescent layer.

[0015] The step of forming an organic electroluminescent layer over the anode layer preferably comprises forming a hole injection layer over the anode layer; forming a hole transport layer over the hole injection layer; forming an emission layer over the hole transport layer; forming an electron transport layer over the emission layer; and forming an electron injection layer over the electron transport layer.

[0016] Another example is an integrated circuit for a pixel. The integrated circuit includes a common electrode layer and an organic light emitting device located on the common electrode layer. The organic light emitting device includes an emission surface. A drive transistor is disposed on part of the emission surface. A reflector layer is disposed between the drive transistor and the organic light emitting device. The

reflector layer includes an aperture over the emission surface and a reflective surface facing the emission surface. The reflective surface reflects light emitted from the light emitting surface through the aperture.

[0017] The foregoing and additional aspects and embodiments of the present invention will be apparent to those of ordinary skill in the art in view of the detailed description of various embodiments and/or aspects, which is made with reference to the drawings, a brief description of which is provided next.

BRIEF DESCRIPTION OF THE DRAWINGS

[0018] The foregoing and other advantages of the invention will become apparent upon reading the following detailed description and upon reference to the drawings.

[0019] FIG. 1A is a layout of a prior art integrated circuit for an OLED pixel;

[0020] FIG. 1B is a circuit diagram of one of the OLEDs and corresponding drive transistor for the OLED pixel in FIG. 1A;

[0021] FIG. 1C is a side view of the integrated circuit of the OLED pixel in FIG. 1A;

[0022] FIG. 2 is a block diagram of an AMOLED display with reference pixels to correct data for parameter compensation control;

[0023] FIG. 3 is a configuration of an integrated circuit for a RGB type pixel having staggered OLEDs for increased aperture;

[0024] FIG. 4 is a configuration of an integrated circuit for a RGBW type pixel having staggered OLEDs for increased aperture;

[0025] FIG. 5 is a configuration of an integrated circuit for a top emission arrangement for an RGB OLED pixel;

[0026] FIG. 6 is an alternate configuration for an integrated circuit for a top emission RGB OLED pixel;

[0027] FIG. 7 is a cross section view of an OLED pixel with a reflector to increase luminance output from the pixel;

[0028] FIG. 8A is a graph of the aperture ratios of a known stripe arrangement of OLEDs in a pixel in comparison with the staggered arrangement in FIG. 3;

[0029] FIG. 8B is a graph of the aperture ratio of known stripe arrangements of OLEDs in a pixel in comparison with a staggered top emission arrangement such as that in FIG. 7; and

[0030] FIGS. 9A-9M are cross-sectional views illustrating the formation of a pixel structure having a high effective aperture ratio according to an embodiment of the invention.

[0031] While the invention is susceptible to various modifications and alternative forms, specific embodiments have been shown by way of example in the drawings and will be described in detail herein. It should be understood, however, that the invention is not intended to be limited to the particular forms disclosed. Rather, the invention is to cover all modifications, equivalents, and alternatives falling within the spirit and scope of the invention as defined by the appended claims.

DETAILED DESCRIPTION

[0032] FIG. 2 is an electronic display system 200 having an active matrix area or pixel array 202 in which an array of active pixels 204a-d are arranged in a row and column configuration. Each of the active pixels 204 includes red, green and blue organic light emitting devices (OLED) to emit different color components that are combined to produce differ-

ent colors for emission from the pixel. For ease of illustration, only two rows and columns of pixels are shown. External to the active matrix area **202** is a peripheral area **206** where peripheral circuitry for driving and controlling the pixel array **202** are located. The peripheral circuitry includes a gate or address driver circuit **208**, a source or data driver circuit **210**, a controller **212**, and an optional supply voltage (e.g., V_{dd}) driver **214**. The controller **212** controls the gate, source, and supply voltage drivers **208**, **210**, **214**. The gate driver circuit **208**, under control of the controller **212**, operates on address or select lines SEL[i], SEL[i+1], and so forth, one for each row of pixels **204** in the pixel array **202**. In pixel sharing configurations described below, the gate or address driver circuit **208** can also optionally operate on global select lines GSEL[j] and optionally /GSEL[j], which operate on multiple rows of pixels **204a-d** in the pixel array **202**, such as every two rows of pixels **204**. The source driver circuit **210**, under control of the controller **212**, operates on voltage data lines Vdata[k], Vdata[k+1], and so forth, one for each column of pixels **204** in the pixel array **202**. The voltage data lines carry voltage programming information to each pixel **204** indicative of brightness of each of the color components of the light emitting devices in the pixel **204**. A storage element, such as a capacitor, in each of the light emitting devices of the pixels **204** stores the voltage programming information until an emission or driving cycle turns on each of the light emitting devices. The optional supply voltage driver **214**, under control of the controller **212**, controls a supply voltage (VDD) line, one for each row of pixels **204** in the pixel array **202**.

[0033] The display system **200** may also include a current source circuit, which supplies a fixed current on current bias lines. In some configurations, a reference current can be supplied to the current source circuit. In such configurations, a current source control controls the timing of the application of a bias current on the current bias lines. In configurations in which the reference current is not supplied to the current source circuit, a current source address driver controls the timing of the application of a bias current on the current bias lines.

[0034] As is known, each pixel **204** in the display system **200** needs to be programmed with data indicating the brightness of each of the light emitting devices in the pixel **204** to produce the desired color to be emitted from the pixel **204**. A frame defines the time period that includes a programming cycle or phase during which each and every pixel **204** in the display system **200** is programmed with programming voltages indicative of a brightness and a driving or emission cycle or phase during which each light emitting device in each pixel is turned on to emit light at a brightness commensurate with the programming voltage stored in a storage element. A frame is thus one of many still images that compose a complete moving picture displayed on the display system **200**. There are at least two schemes for programming and driving the pixels: row-by-row, or frame-by-frame. In row-by-row programming, a row of pixels is programmed and then driven before the next row of pixels is programmed and driven. In frame-by-frame programming, all rows of pixels in the display system **200** are programmed first, and all of the pixels are driven row-by-row. Either scheme can employ a brief vertical blanking time at the beginning or end of each frame during which the pixels are neither programmed nor driven.

[0035] The components located outside of the pixel array **202** may be located in a peripheral area **206** around the pixel array **202** on the same physical substrate on which the pixel

array **202** is disposed. These components include the gate driver **208**, the source driver **210** and the optional supply voltage control **214**. Alternately, some of the components in the peripheral area can be disposed on the same substrate as the pixel array **202** while other components are disposed on a different substrate, or all of the components in the peripheral area can be disposed on a substrate different from the substrate on which the pixel array **202** is disposed. Together, the gate driver **208**, the source driver **210**, and the supply voltage control **214** make up a display driver circuit. The display driver circuit in some configurations may include the gate driver **208** and the source driver **210** but not the supply voltage control **214**.

[0036] The display system **200** further includes a current supply and readout circuit **220**, which reads output data from data output lines, VD[k], VD[k+1], and so forth, one for each column of pixels **204a**, **204c** in the pixel array **202**. The drive transistors for the OLEDs in the pixels **204** in this example are thin film transistors that are fabricated from amorphous silicon. Alternatively, the drive transistors may be fabricated from polysilicon.

[0037] In the configurations for the OLEDs described below, the aperture ratio is improved through minimizing the blocked area of the OLED emission surface by changing the arrangement of the drive transistors and the OLEDs. Another configuration for top emission allows the light guided from the area that is blocked by the drive transistor and metallic layers such as power and programming lines to a window over the emission surface of the OLED. As a result, the aperture ratio is much larger than actual opening.

[0038] The arrangement of OLED and drive transistors described below makes the pixel opening less dependent to the fabrication design rules that require certain distances between OLEDs and certain widths of voltage supply and data lines. This technique allows fabrication of high resolution displays while results in reasonable aperture ratio without the need for a high resolution fabrication process. Consequently, the use of shadow masks becomes possible, or even easier, for partitioning the pixel for high pixel densities.

[0039] FIG. 3 shows a top view of an integrated circuit layout for a pixel **300** which is a staggered architecture for a RGB bottom emission pixel. The integrated circuit layout of the pixel **300** includes a top subrow **302** and a bottom subrow **304** each having a series of OLEDs. Each of the OLEDs constitute a sub-pixel in the individual pixels such as the pixel **300**. The sub-pixels (e.g. green, red and blue) alternate between the subrows. In this example, the top subrow **302** includes a green OLED **310**, a drive transistor **312**, a red OLED **314** and a drive transistor **316**. The bottom subrow **304** includes a drive transistor **320**, a blue OLED **322**, a drive transistor **324** and a green OLED **326**. A select line **330** is fabricated on top of the top subrow **302** and a select line **332** is fabricated on the bottom of the bottom subrow **304**. The drive transistor **316** and the green OLED **326** belong to a next pixel **350** in the array and share the select lines **330** and **332** with the pixel **300**. The OLEDs **310**, **314** and **322** in the pixel **300** are therefore in staggered arrangement allowing them to be placed closer together side by side. It is to be understood that the term subrow is simply used for convenience. From another perspective, the different OLEDs may be staggered on adjacent columns. The various OLEDs are arranged so certain OLEDs are next to each other and other OLEDs are above or below the OLEDs next to each other in order to allow the increase in the width of the OLEDs.

[0040] A power line 340 borders both the green OLED 310 and the drive transistor 320. A data line 342 is fabricated between the green OLED 310 and the drive transistor 312 of the top subrow 302 and continues between the drive transistor 320 and the blue OLED 322 of the bottom subrow 304. A power line 344 is fabricated between the drive transistor 312 and the red OLED 314 of the top subrow 302 and continues between the blue OLED 322 and the drive transistor 324 of the bottom subrow 304. The structure of the pixel 300 also includes a data line 346 fabricated between the red OLED 314 and the drive transistor 314 of the top subrow 302 and continues between the transistor 324 and the green OLED 326 of the bottom subrow 304. Another power line 348 borders the drive transistor 316 of the top subrow 302 and the green OLED 326 of the bottom subrow 304. The drive transistor 316 and the green OLED 326 are part of the next pixel 350 adjacent to the pixel 300 but share the data line 346.

[0041] In FIG. 3, the display circuit of the pixel 300 is divided into the two subrows 302 and 304. The OLEDs 310, 322 and 314 are put on top and bottom side of the pixel area alternatively. As a result, the distance between two adjacent OLEDs will be larger than the minimum required distance. Also, the data lines such as the data lines 342 and 346 may be shared between two adjacent pixels such as the pixel 300 and the adjacent pixel 350. This results in a large aperture ratio because the distance between the OLEDs such as the OLED 310 and the OLED 322 may be reduced due to the staggered configuration resulting in larger emission areas of the OLEDs. Since the OLEDs in the pixel 300 share power lines, the surface area necessary for such lines is reduced allowing the area to be open to the emission surfaces of the OLEDs therefore further increasing the aperture ratio.

[0042] FIG. 4 shows an example staggered architecture for a RGBW bottom emission display pixel circuit 400. The integrated circuit layout for the pixel 400 includes a top subrow 402 and a bottom subrow 404. In this example, the top subrow 402 includes a green OLED 410, a drive transistor 412, a red OLED 414 and a drive transistor 416. The bottom subrow 404 includes a drive transistor 420, a blue OLED 422, a drive transistor 424 and a white OLED 426. FIG. 4 shows the entire pixel which includes the four OLEDs 410, 414, 422 and 426.

[0043] A select line 430 is fabricated on top of the top subrow 402 and a select line 432 is fabricated on the bottom of the bottom subrow 404. A power line 440 borders both the green OLED 410 and the drive transistor 420. A data line 442 is fabricated between the green OLED 410 and the drive transistor 412 of the top subrow 402 and continues between the drive transistor 420 and the blue OLED 422 of the bottom subrow 404. A power line 444 is fabricated between the drive transistor 412 and the red OLED 414 of the top subrow 402 and continues between the blue OLED 422 and the drive transistor 424 of the bottom subrow 404. The circuit 400 also includes a data line 446 fabricated between the red OLED 414 and the drive transistor 416 of the top subrow 402 and continues between the drive transistor 424 and the white OLED 426 of the bottom subrow 404. Another power line 448 borders the drive transistor 416 of the top subrow 402 and the white OLED 426 of the bottom subrow 404. The power lines 440 and 448 are shared by adjacent pixels (not shown).

[0044] As with the configuration in FIG. 3, the pixel circuit 400 in FIG. 4 has increased aperture because the distance between parallel OLEDs may be decreased due to the staggered relationship between the OLEDs 410, 414, 422 and

426. The white OLED 426 is added since most of the display using the pixel circuit 400 typically emits white color and the white OLED 426 reduces continuous emissions from the blue OLED 422 which is primarily employed to emit white color in RGB type pixels such as the pixel 300 in FIG. 3. As with the configuration in FIG. 3, the distances between the OLEDs may be decreased resulting in greater exposure of the emission surface areas. Further, the sharing of the data and power supply lines also reduces the area necessary for such lines resulting in additional surface emission area being exposed for the OLEDs.

[0045] The same staggered arrangement as shown in FIGS. 3 and 4 may be used for the top emission type OLED integrated circuit. FIG. 5 shows a staggered color patterning for a RGB top-emission display structure 500. The structure 500 includes a top subrow 502 and a bottom subrow 504. The top subrow 502 includes a green OLED 512 and a red OLED 514. The drive transistors to drive the OLEDs 512 and 514 are mounted on a lower circuit layer 516 under the OLEDs 512 and 514. The bottom subrow 504 includes a blue OLED 522 and a green OLED 524. Drive transistors that drive the OLEDs 522 and 524 are fabricated on a circuit layer 526 under the OLEDs 522 and 524. In the display structure 500, the OLEDs 512, 514 and 522 make up one pixel, while the green OLED 524 is part of another pixel. Thus the structure 500 results in a display with interlocked pixels which share various data lines. Such pixels require some interpolation of image data since the data lines are shared between the OLEDs of the pixels.

[0046] A select line 530 is fabricated on top of the top subrow 502 and a select line 532 is fabricated on the bottom of the bottom subrow 504. A power line 540 borders both the green OLED 510 and the blue OLED 520. A data line 542 is fabricated under the green OLED 510 and of the top subrow 502 and continues under the blue OLED 522 of the bottom subrow 504. The data line 542 is used to program the green OLED 512 and the blue OLED 522. A power line 544 is fabricated between the green OLED 512 and the red OLED 514 of the top subrow 502 and continues between the blue OLED 522 and the green OLED 524 of the bottom subrow 504. A data line 546 fabricated over the red OLED 514 of the top subrow 502 and continues over the green OLED 524 of the bottom subrow 404. The data line 546 is used to program the red OLED 514 and the green OLED 524. Another power line 548 borders the red OLED 514 of the top subrow 502 and the green OLED 524 of the bottom subrow 504. The power lines 540 and 548 are shared by the transistors and OLEDs of adjacent pixels.

[0047] In this case, sharing the data programming lines 542 and 546 (VDATA) in the top emission structure 500 leads to more area for the drive transistors under the OLEDs. As a result, the drive transistors in the emission structure 500 may have larger source, drain and gate regions and the aging of the drive transistors will be slower because of lower current densities required by the transistors.

[0048] The emission structure 500 allows reduction of distance between the OLEDs 512 and 522 because of the staggered arrangement. The OLEDs 512, 514, 522 and 524 may be made wider than a known OLED, but with a relatively shorter length. The wider OLED surface results in increased aperture ratio. The emission structure 500 requires a processed image data signal from a raw RGB signal because the OLEDs are staggered with OLEDs from the adjacent pixels. The transparent common electrode (not shown) over the

OLEDs 512, 514, 522 and 524 has relatively lower resistance because of the wider areas of the OLEDs 512, 514, 522 and 524.

[0049] FIG. 6 shows an alternate pixel arrangement 600 for a top emission structure. The pixel arrangement 600 improves the aperture ratio and relaxes OLED manufacturing requirements. The pixel arrangement 600 includes different pixels 602, 604, 606 and 608. Each of the pixels has three OLEDs such as OLEDs 610, 612 and 614 which are disposed on a circuit layer 616 that includes the drive transistors to drive each of the OLEDs 610, 612 and 614. In this case, the OLED 610 emits green light and is in a row with the OLED 612 that emits red light. The OLED 614 emits a blue light and has a larger emission surface than the OLEDs 610 and 612. Select lines such as select lines 620, 622 and 624 run on the top and the bottom of the pixels 602, 604, 606 and 608. Power supply lines 630, 632 and 634 run along the sides of the pixels 602, 604, 606 and 608 to supply voltages for the OLEDs 610, 612 and 614 and their respective drive transistors. Data lines 640, 642, 644 and 646 run under the OLEDs of the pixels 602, 604, 606 and 608. For example, the data line 640 is used to program the OLED 610, the data line 642 is used to program the OLED 612 and either data line 640 or 644 is used to program the OLED 614 in the pixel 602.

[0050] In the structure 600, any single current is within one sub-row. As a result, the lines look straighter in a display composed of pixels using the arrangement 600 and so provide better quality for text application. The OLED 614 that emits blue light is larger than the OLEDs 610 and 612, covering substantially the entire width of the pixel 602, because the increased surface area for the blue color OLED 614 retards aging which is the result of inherent faster aging for a blue color OLED. The increased surface area requires lower current density to produce the same output as a smaller surface OLED and therefore ages slower. The structure 600 in FIG. 6 has an improved appearance over the structure 500 in FIG. 5 because the red, green and blue OLED elements are in a straight line as opposed to being staggered between pixels. As with the structure 500 in FIG. 5, the transparent common electrode (not shown) over the OLEDs 610, 612 and 614 has relatively lower resistance because of the wider areas of the OLEDs 610, 612 and 614, as shown in FIG. 9E.

[0051] FIG. 7 shows the cross section of a pixel structure 700 that is a modified bottom emission type pixel that increases aperture ratio by having a reflector focus light emitted from the areas of the emission area of an OLED 702 that are covered by other circuit components. The OLED 702 includes a cathode layer 704 and an anode layer 706. A common electrode layer 708 provides electrical bias to the other side of the OLED 702. The common electrode 708 can be shaped as a concave mirror to reflect more light toward the reflective surface 740. A drive transistor 710 is fabricated over part of the emission surface of the OLED 702. The drive transistor 710 includes a gate 712, a drain region 714 and a source region 716. The drive transistor 710 is fabricated on a clear substrate layer 720 that overlays the OLED 702. A metallization layer 730 is overlaid on the clear substrate 720 to form electrodes 732 and 734 contacting the drain region 714 and the source region 716 of the drive transistor 710 respectively and provide electrical connections to the other components of the circuit such as data and voltage supply lines. An electrode (not shown) is also formed to the gate of the transistor 710. The metallization layer 730 includes an

aperture 736 through which light from the OLED 702 may be emitted through the clear substrate 720.

[0052] The pixel structure includes a reflector 740 that is disposed between the OLED 702 and the drive transistor 710. The reflector 740 includes a reflective surface 742 facing the emission surface of the OLED 702 that reflects light emitted from the OLED 702 that would be normally blocked by the drive transistor 710. The reflected light (shown in arrows in FIG. 7) is emitted out a window 744 in the reflector 740 to therefore increase the light actually emitted from the OLED 702.

[0053] Thus the OLED emission area is not limited to the opening window which is defined by the drive transistor and supporting components on the OLED 702. As a result, the OLED current density for a given luminance is lower than a conventional bottom emission arrangement. This arrangement including the reflector 740 requires lower OLED voltage and therefore lower power consumption to achieve the same luminance as a conventional OLED without the reflector. Moreover, the lifetime of the OLED 702 will be longer due to lower current density. This structure 700 may also be used with other techniques to further improve aperture ratio.

[0054] The aperture ratio for different display resolutions is demonstrated in a graph 800 in FIG. 8A. The graph 800 compares the aperture ratios of various configurations to display resolutions. One set of data points 802 shows the aperture ratios of a standard amorphous silicon red green blue pixel stripe structure as shown in FIG. 1A. A second set of data points 804 shows the aperture ratios of a standard polysilicon red green blue pixel stripe structure. As shown in FIG. 8A, the polysilicon based pixel has slightly better aperture ratios than the amorphous silicon based pixel. A third set of data points 806 shows the aperture ratios of a bottom emission staggered structure such as the structure of the pixel 300 shown in FIG. 3. As shown in the data points 802 in FIG. 8A, while the aperture ratio for higher resolution (e.g., 250 PPI) using a standard RGB stripe configuration is zero, the aperture ratio of the staggered pixel architecture in FIG. 3 in data points 806 is higher than 20% for up to 260 PPI.

[0055] FIG. 8B is a graph 850 showing the plots of aperture ratios at different display resolutions for various OLED pixel structures. One set of data points 852 shows the aperture ratios of a standard amorphous silicon red green blue pixel stripe structure as shown in FIG. 1A fabricated with a shadow mask. A second set of data points 854 shows the aperture ratios of an amorphous silicon bottom emission staggered structure such as the structure of the pixel 300 shown in FIG. 3 fabricated with a shadow mask. Another set of data points 856 shows the aperture ratios of a top emission type structure in a red green blue pixel strip structure fabricated by laser induced thermal imaging (LITI). A final set of data points 858 shows the aperture ratios of a top emission type structure using the staggered arrangement shown in FIG. 7 fabricated by LITI.

[0056] The aperture ratio is extracted for two types of OLED patterning (shadow mask with a 20- μ m gap and LITI with a 10- μ m gap) as shown in the data points 852 and 856 for a stripe type arrangement as shown in FIG. 1A. In the case of shadow mask fabrication, the aperture ratio for RGB stripe is limited by OLED design rules whereas a RGB stripe using LITI fabrication is limited by the TFT design rules. However, for both shadow mask and LITI fabrication, staggered color patterning can provide high resolution (e.g. 300 ppi) with large aperture ratio as shown by the data points 854 and 858.

This resolution is provided without mandating tighter design rules as compared with conventional OLED layouts.

[0057] A preferred method of fabricating the pixel structure described above by (1) forming a first photoresist layer with the first opening **736** on the substrate **720**, forming the reflective layer **740** with the second opening **744** over the first photoresist layer, forming a second photoresist layer in the opening **744** and over the reflective layer; and forming the organic light emitting device **702** over the second photoresist layer. The second opening **744** overlaps the first opening **736**, and at least a portion of the reflective layer **740** is concave in shape. The transistor elements **710**, **712**, **714**, **716**, **732** and **734** are formed on the surface of the substrate **720** below the reflective layer, offset from the openings **736** and **744**.

[0058] FIGS. 9A-9M are cross-sectional views illustrating successive steps of one exemplary fabrication process for a pixel structure having a high effective aperture ratio according to an embodiment of the invention. These steps can be used to manufacture a pixel structure as shown. The pixel structure is a modified bottom emission type pixel that increases effective aperture ratio, such that the effective aperture ratio is larger than the actual aperture ratio of the device. For simplicity of description, the transistor circuits supporting the pixel structure are omitted. However, it is contemplated that the pixel structure of FIGS. 9A-9M can include one or more supporting transistors (e.g., TFTs), such as drive transistor **710** and its associated components, positioned as shown in FIG. 7.

[0059] A substrate **910** is provided. Substrate **910** may be, for example, a glass wafer. Substrate **910** is cleaned with an RCA solution; specifically, a 1:1:5 solution of NH_4OH (ammonium hydroxide), H_2O_2 (hydrogen peroxide), and H_2O (water), respectively. Substrate **910** is cleaned with the solution at 80°C . for 20 minutes.

[0060] A first photoresist layer **915** is formed to a thickness of $11.6\ \mu\text{m}$ on substrate **910**, as shown in FIG. 9A. In this embodiment, first photoresist layer **915** is spin coated on substrate **910** at 800 rpm for 10 seconds, then at 4000 rpm for 60 seconds. First photoresist layer **915** may comprise any suitable transparent photoresist material, such as, for example, SU-8 photoresist. In another embodiment, first photoresist layer **915** comprises a black or dark polymer. First photoresist layer **915** is then soft baked at 95°C . for 3 minutes, exposed for 16 seconds, and hard baked at 95°C . for 4 minutes.

[0061] Next, as shown in FIG. 9B, a mask layer **920** is formed to a thickness of 100 nm on first photoresist layer **915**. Mask layer **920** is used as a hard mask for later etching of first photoresist layer **915** and can be, for example, an aluminum film. In this embodiment, mask layer **920** is deposited using WLOS sputtering with 50 sccm Ar, 9 mTorr pressure, 300 W DC power, and 700 seconds deposition time.

[0062] A second photoresist layer **925** is formed on mask layer **920** for photolithography, as shown in FIG. 9C. In this embodiment, second photoresist layer **925** is spin coated on mask layer **920** at 500 rpm for 10 seconds, then at 4000 rpm for 60 seconds. Second photoresist layer **925** may comprise any suitable photoresist material such as, for example, AZ3312 photoresist. Second photoresist layer **925** is then soft baked at 90°C . for 1 minute.

[0063] Photo mask **930a-c** is then applied to second photoresist layer **925**, and ultraviolet (UV) exposure is applied from the top (i.e., on the side of photo mask **930a-c**), as shown in FIG. 9D. In this embodiment, UV exposure is maintained

for 4 seconds with an intensity of $10\ \text{mW}/\text{cm}^2$. AZ 300 MIF developer is then applied and developed for 16 seconds, and the sample is post-exposure baked at 120°C . for 60 seconds, resulting in separate second photoresist layers **925a** and **925b**.

[0064] As shown in FIG. 9F, mask layer **920** is etched into separate mask layers **920a** and **920b**. In this embodiment, mask layer **920** is etched using a polyacrylonitrile (PAN) solution; specifically, a 16:2:1:1 solution of H_3PO_4 (phosphoric acid), H_2O (deionized water), HAc (acetic acid), and HNO_3 (nitric acid), respectively, is used. Mask layer **920** is etched at 40°C . for 3-4 minutes. Then, second photoresist layers **925a** and **925b** are removed. In this embodiment, second photoresist layers **925a** and **925b** are removed using acetone or AZ300 stripper.

[0065] First photoresist layer **915** is then etched into separate first photoresist layers **915a**, **915b**, as shown in FIG. 9G, forming a concave shape. In this embodiment, first photoresist layer is isotropically dry etched using inductively coupled plasma (ICP). The ICP dry etching recipe is: 20 O_2 , 2 CF_4 , 180 ICP power, 50 pressure, and 700 seconds etching time. As shown in FIG. 9H, separate mask layers **920a** and **920b** are removed. In this embodiment, separate mask layers **920a** and **920b** are removed using a polyacrylonitrile (PAN) solution.

[0066] Reflective layer **940** is then deposited, as shown in FIG. 9I. In this embodiment, reflective layer **940** is deposited using WLOS sputtering with 50 sccm Ar, 9 mTorr pressure, 300 W DC power, and 700 seconds deposition time. As shown in FIG. 9J, the emission windows are then opened using photolithography. A third photoresist layer (not shown) is spin coated at 3000 rpm for 30 seconds, soft baked at 100°C . for 6 minutes, then re-hydrated for 30 minutes. The third photoresist layer can comprise any suitable photoresist layer, and in this embodiment, comprises AZ P4330 photoresist. The third photoresist layer is then exposed to 365 nm ultraviolet radiation for 35 seconds, and developed in a 1:4 solution of AZ400K developer and deionized water, respectively, for 6 minutes. The portion of mirror layer **940** on substrate **910** is then etched with polyacrylonitrile for 4 minutes, resulting in separate mirror layers **940a** and **940b**, and the rest of the third photoresist layer is removed using stripper.

[0067] As shown in FIG. 9K, a fourth photoresist layer **945** is deposited in the opening of mirror layers **940a** and **940b**, and over reflective layers **940a** and **940b**. In this embodiment, fourth photoresist layer **945** is spin coated at 800 rpm for 10 seconds, then at 4000 rpm for 60 seconds. Fourth photoresist layer **945** may comprise any suitable transparent photoresist material, such as, for example, SU-8 photoresist. Fourth photoresist layer **945** is then soft baked at 95°C . for 3 minutes, exposed for 16 seconds, and hard baked at 95°C . for 4 minutes.

[0068] Anode **950** is then deposited over fourth photoresist layer **945**, as shown in FIG. 9L. In this embodiment, anode **950** is an indium tin oxide (ITO) film. Anode **950** is deposited using an AJA sputtering system with a ratio of $\text{Ar}:\text{O}_2$ of 16:0.5, a temperature of 150°C ., RF power of 100 W, and deposition time of 50 minutes. Post-annealing is then conducted at 150°C . for 30 minutes. Anode **950** can then be patterned using another photolithography process.

[0069] OLEDs are then deposited on top of the patterned anode **950**, as shown in FIG. 9M. In this embodiment, the OLEDs are deposited using an Intevoc thermal evaporation system at a pressure under 5×10^{-6} Torr. The OLEDs comprise

anode **950**, organic electroluminescent layer **955**, and cathode **960**. A common electrode layer (not shown) can be formed over cathode **960**.

[0070] As appreciated by one skilled in the art, organic electroluminescent layer **955** can comprise a plurality of layers, including (from anode **950** to cathode **960**) a hole injection layer, a hole transport layer, an emission layer, an electron transport layer and an electron injection layer. In one embodiment, the hole injection layer comprises MoO_3 ; the hole transport layer comprises NPB; the electron transport layer comprises Alq_3 ; the electron injection layer comprises LiF; and cathode **960** comprises Al.

[0071] The pixel structure includes reflective layers **940a**, **940b** that are disposed between the OLED (comprising anode **950**, organic electroluminescent layer **955**, and cathode **960**) and the drive transistor(s) (not shown, but positioned between the substrate and first photoresist layers **915a** and **915b**). Reflective layers **940a**, **940b** include a reflective surface facing the emission surface of the OLED that reflects light emitted from the OLED that would be normally blocked by the drive transistor(s). The reflected light is emitted out an opening between mirror layers **940a** and **940b** to therefore increase the light actually emitted from the OLED. Because of the concave shape of reflective layers **940a** and **940b**, reflected light (as well as ambient light) is guided toward the opening between reflective layers **940a** and **940b**.

[0072] Thus, the OLED emission area is not limited to the opening window which is defined by the drive transistor and supporting components on the OLED. As a result, the OLED current density for a given luminance is lower than a conven-

tional bottom emission arrangement. This arrangement including reflective layers **940a**, **940b** requires lower OLED voltage and therefore lower power consumption to achieve the same luminance as a convention OLED without the mirror layers. Moreover, the lifetime of the OLED will be longer due to lower current density. This structure may also be used with other techniques to further improve effective aperture ratio.

[0073] While particular embodiments and applications of the present invention have been illustrated and described, it is to be understood that the invention is not limited to the precise construction and compositions disclosed herein and that various modifications, changes, and variations can be apparent from the foregoing descriptions without departing from the spirit and scope of the invention as defined in the appended claims.

1-13. (canceled)

14. A color display comprising:

a controller;

an array of pixels coupled to the controller to display images and including:

organic light emitting devices of alternating first and second colors located in every other row and every other column,

an organic light emitting device of a third color located in intervening rows and intervening columns, and

first, second and third drive transistors coupled to said organic light emitting devices of said first, second and third colors, respectively.

* * * * *

专利名称(译)	高分辨率像素架构		
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[标]申请(专利权)人(译)	伊格尼斯创新公司		
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摘要(译)

像素结构包括基本上透明的基板，形成在基板上的驱动晶体管，形成在驱动晶体管的与基板相对的一侧上的有机发光器件，设置在发光器件和驱动晶体管之间的反射层面向发光器件的反射表面。反射层形成偏离驱动晶体管的开口，用于将发光器件发射的光传递到基板。至少一部分反射层优选为凹形，以将来自发光装置的反射光引导回到发光装置上。

